In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended): A semiconductor configuration for dissipating heat away from a semiconductor device having a plurality of power lines, the configuration comprising:

a semiconductor substrate; and

a plurality of interconnect structures disposed on the substrate and in contact therewith and extending through the semiconductor device, the interconnect structures for dissipating heat through the substrate,

wherein the plurality of interconnect structures are disposed within a power line.

2. (original): The semiconductor configuration of claim 1, further comprising a heat sink in contact with the substrate.

3. (original): The semiconductor configuration of claim 1, wherein each of the plurality of interconnect structures comprises at least one via stack.

4. (currently amended): The semiconductor configuration of claim 3, wherein the plurality of interconnect structures are closed to the power line.

5. (original): The semiconductor configuration of claim 3, wherein at least one of the plurality of interconnect structures is joined to one other of the plurality of interconnect structures using a bridge structure.

6. (original): The semiconductor configuration of claim 3, including bridge structures, each of the bridge structures joins a respective one of the plurality of interconnect structures to one other of the plurality of interconnect structures.

7. (original): The semiconductor configuration of claim 3, wherein a width of each of the interconnect structures is from about 0.1μm to about 10μm.

8. (original): The semiconductor configuration of claim 3, wherein the interconnect structures are spaced apart from each other by a width of one of the interconnect structures.

9. (original): The semiconductor configuration of claim 3, wherein each of the plurality of bridges is alternatively spaced apart from a serpentine power line by a distance.

10. (original): The semiconductor configuration of claim 9, wherein the distance is a width of one of the plurality of interconnect structures.

11. (original): The semiconductor configuration of claim 3, wherein each of the plurality of interconnect structures is spaced apart from a linear power line by a distance.

12. (original): The semiconductor configuration of claim 11, wherein the distance is the width of one of the plurality of interconnect structures.

13. (currently amended): The semiconductor configuration of claim 3, wherein ~~the plurality of interconnect structures are disposed within a power line,~~ the plurality of interconnect structures are substantially enveloped in a dielectric film.

14. (original): The semiconductor configuration of claim 13, wherein the interconnect structures are alternatively spaced apart from each other by a width of one of the interconnect structures.

15. (original): The semiconductor configuration of claim 13, wherein a ratio of the width of one of the interconnect structures to the power line is between about 1 to about 20.

16. (original): The semiconductor configuration of claim 13, wherein a width of each of the interconnect structures is from about 0.1μm to about 10μm.

17. (original): The semiconductor configuration of claim 13, wherein the interconnect structures are spaced apart from each other by a width of one of the interconnect structures.

18. (original): The semiconductor configuration of claim 13, wherein each of the plurality of interconnect structures is alternatively spaced apart within the power line by a distance.

19. (original): The semiconductor configuration of claim 18, wherein the distance is the width of one of the plurality of interconnect structures.

20. (original): The semiconductor configuration of claim 13, wherein the power line has a serpentine shape.

21. (original): The semiconductor configuration of claim 13, wherein the power line has a linear shape.

22. (currently amended): A semiconductor configuration for dissipating heat away from a semiconductor device having a plurality of power bus lines, comprising:

a semiconductor substrate; and

a plurality of interconnect structures, each of the interconnect structures having at least one via stack, the interconnect structures disposed on the substrate and in contact therewith and extending through the semiconductor device, the interconnect structures for dissipating heat through the substrate,

wherein each of the plurality of bridges is alternatively spaced apart from a serpentine power line by a distance.

23. (currently amended): A semiconductor configuration for dissipating heat away from a semiconductor device having a plurality of power lines, comprising:

a semiconductor substrate; and

a plurality of interconnect structures disposed on the substrate and in contact therewith and extending through the semiconductor device, the interconnect structures for dissipating heat through the substrate,

wherein the plurality of interconnect structures are periodically spaced apart along a longitudinal axis of the plurality of power lines by a distance.

24. (currently amended): A method for forming a semiconductor configuration for dissipating heat away from a semiconductor device having a plurality of power bus lines, comprising:

providing a semiconductor substrate; and

forming a plurality of interconnect structures disposed on the substrate and in contact therewith and extending through the semiconductor device, the interconnect structures for dissipating heat through the substrate,

wherein the plurality of interconnect structures are formed within the plurality of power bus lines.

25. (original): The method of claim 24, further comprising providing a heat sink in contact with the substrate.